IP-CORE SOLUTION

X-PROTOCOL

CLHS IP Core Purchase

INTRODUCTION

The Camera Link HS® IP-Core solution is a group of FPGA ready cores implementing the message layer of the Camera Link HS standard.

The solution provides cores for both camera and frame grabber devices for the X-Protocol. It can be used on Altera and Xilinx FPGA but can be easily extended to other FPGA technologies.

APPLICATIONS

Figure 1 shows a one lane X-Protocol Camera Link HS architecture. The Camera Link HS Camera and Frame Grabber module IP cores bridge the User's logic to/from an XGMII interface. These modules perform priority and packet formation and packet unpacking. The Module inputs and outputs can be connected to the CLHS PCS or directly to a serdes that supports 10GBASE-R to perform the 64/66b encoding and addition of Forward Error Correction as specified in IEEE 802.3ae-Clause 74. The CLHS discovery process occurs at 10.3125 Gbps and can be negotiated to 25.78125 Gbps if both ends support the bit rate. The X protocol also supports 12.5, 13.75 and 15.94 Gbps rates.

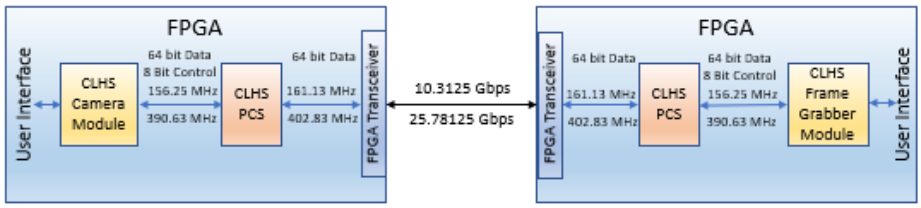

Figure 1: Typical X-Protocol Camera Link HS device architecture

FEATURES

- Full bridge between the CLHS Message Interface and a 10Gbs Ethernet PCS/PMA core
- Compliant with revision 1.0 of the CLHS standard
- Implements the full CLHS message layer with packet priority engine
- Simple signaling user interface
- VHDL-93 RTL format
- Both camera and frame grabber cores included

FPGAs

- Xilinx
- Altera
- Easy to extend to other FPGA architectures

SIMULATION

- VHDL/Java test-bench
- Modelsim simulator

DOCUMENTATION

- Core user guide
- Validation user guide

VISION & IMAGING

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FUNCTIONAL OVERVIEW

Figure 2 illustrates the Camera Link HS XP-Core block diagram for both a camera and a frame grabber. Each sub-module is composed of a packetizer engine and a de-packetizer engine. The packetizer engine is a module responsible of converting Camera Link HS message information into packets and requesting access to the link through the priority engine. The priority engine is responsible of granting the link access to each packetizer according to the message priority. Interrupted packets resume transmission under the control of the priority engine.

On the receiver side the DEMUX logic is responsible of routing arriving packets on the link to the corresponding message de-packetizer.

The camera and the frame grabber core differ only in the packetizer for video messages; the camera provides only a video packetizer while the frame grabber has only a video de-packetizer.

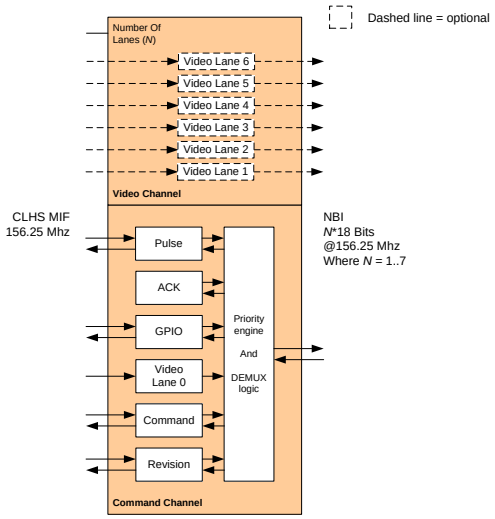

Figure 2: Camera and frame grabber X-Protocol core

All core interfaces are running at a clock frequency of 156.25MHz for a 10.3 Gbps bit rate, except for the video and the command message interfaces which are running on their respective clock domain. The video and command clock must be provided by the user logic. Clock domains crossing are accomplished inside the cores through double clock ram buffers. XP-Cores do not include any clock management logic.

RESOURCES USAGE

The following table provides indicative resources usage of both versions of the core.

Resources	Camera core	Frame grabber core
LUTs	3248	3164
FFs	2789	2699
Block Rams	7	7

Note: based on a Xilinx Virtex-5 device

VERIFICATION

Both X-Protocol cores have been verified through extensive simulations by the Camera Link HS committee members. The complete Camera Link HS validation framework is delivered with the core. However in order to use the validation framework, ModelSim PE and a version of the free Eclipse IDE for Java Developers are required.

The cores have also been tested on real hardware.

SUPPORT

The Camera Link HS IP-Core solution is the result of a volunteer collective development effort by the Camera Link HS community. Fees charged when buying the core are for hosting and advertisement only. The core comes with no warranty and support is only provided on a voluntary basis by the Camera Link HS community.

DELIVERABLES

The X-Protocol cores solution includes all the required parts for a successful implementation:

- VHDL-93 RTL source code
- Complete validation framework based on behavioral VHDL/Java models
- IP-Core instantiation user guide
- Validation user guide
- Free access to bug fixes, optimizations and feature improvements.

ORDERING INFORMATION

The core can be purchased directly from the A3. Visit www.automate.org for more information or use QR code below.

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