IP-CORE SOLUTION

M-PROTOCOL

CLHS IP Core Purchase

INTRODUCTION

The Camera Link HS® IP-Core solution is a group of FPGA ready cores implementing the message layer of the Camera Link HS standard.

The solution provides cores for both camera and frame grabber devices for the M-Protocol. It can be used on Altera and Xilinx FPGA but can be easily extended to other FPGA technologies.

APPLICATIONS

Figure 1 shows a typical Camera Link HS C2, 7M1 M-Protocol (MP) system architecture. This system includes a camera, a frame grabber and a link that based on a standard CX4 cable which provides 1 full-duplex command channel on lane 0 and 6 extra data lanes for a total video bandwidth of 2.1GB/s.

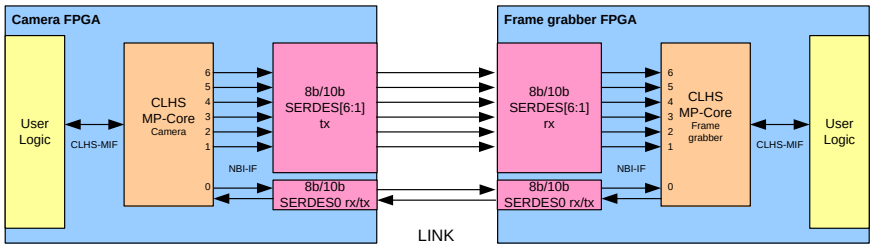

Figure 1: Typical Camera Link HS M-Protocol C2, 7M1 system architecture

In both camera and frame grabber FPGA the M-Protocol is implemented using the respective MP-Core and SERDES. However use of external transmitters is also possible as a replacement to the FPGA SERDES for implementing the complete the M-Protocol solution.

The user logic connects to the Core through the standard Camera Link HS Message Interface (MIF). This interface implements a simple and well define signaling scheme. The interface between the MP-Core and each SERDES is a simple Nine Bit Interface (NBI); 8 bits are for data plus one control bit.

FEATURES

- Full bridge between the CLHS Message Interface and the Nine Bit Interface (NBI)
- Compliant with revision 1.0 of the CLHS standard
- Implements the full CLHS message layer with packet priority engine
- Configurable number of data lane (1 to 7) for a video bandwidth up to 2.1GB/s
- Resend mechanism
- Simple signaling user interface
- VHDL-93 RTL source code
- Both camera and frame grabber cores included

FPGAs

- Xilinx
- Altera
- Easy to extend to other FPGA architectures

SIMULATION

- VHDL/Java test-bench
- Modelsim simulator

DOCUMENTATION

- Core and Validation user guides

FUNCTIONAL OVERVIEW

Figure 2 illustrates the Camera Link HS Camera MP-Core block diagram. It is divided in 2 sections: the command channel and the video channel. The command channel is responsible for sending and receiving all Camera Link HS message types including video. This section is always present in the core. The video channel is optional and can be configured to instantiate from none to 6 extra video lanes.

Each command channel sub-module is composed of a packetizer engine and a de-packetizer engine. A packetizer engine is responsible of converting Camera Link HS message information into packets and requesting access to the link through the priority engine. The priority engine is responsible for granting the link access to each packetizer according to the message priority. Interrupted packets resume transmission under the control of the priority engine. On the receiver side the DEMUX logic is responsible for routing arriving packets on the link to the corresponding message de-packetizer. The de-packetizer is responsible for presenting the received message on the user interface.

The camera and the frame grabber core differ only in the logic for video messages; the camera provides only video packetizers while the frame grabber has only video de-packetizers.

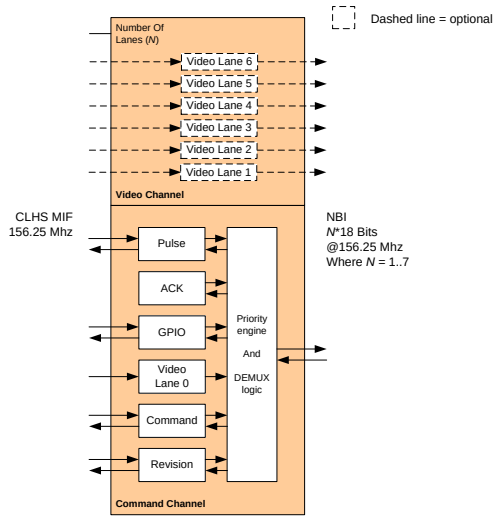

Figure 2: Camera M-Protocol core

All core interfaces are running at a clock frequency of 156.25MHz except for the video and the command message interfaces which are running on their respective clock domain. The video and command clock must be provided by the user logic. MP-Cores do not include any clock management logic. Clock domains crossing are accomplished inside the cores through double clock ram buffers.

RESOURCES USAGE

The following table provides indicative resources usage for 7 lanes and 8KB video message payload.

Resources	Camera core	Frame grabber core
LUTs	4839	8269
FFs	5120	10979
Block Rams	57	113

Note: based on a Virtex 5 device.

VERIFICATION

Both M-Protocol cores have been verified through extensive simulations by the Camera Link HS committee members. The complete Camera Link HS validation framework is delivered with the core. However in order to use the validation framework, *ModelSim PE* and a version of the free *Eclipse IDE for Java Developers* are required. The cores have also been tested on real hardware.

SUPPORT

The Camera Link HS IP-Core solution is the result of a volunteer collective development effort by the Camera Link HS community. Fees charged when buying the core are for hosting and advertisement only. The core comes with no warranty and support is only provided on a voluntary basis by the Camera Link HS community.

DELIVERABLES

The M-Protocol cores solution includes all the required parts for a successful implementation:

- VHDL-93 RTL source code
- Complete validation framework based on behavioral VHDL/Java models
- IP-Core instantiation user guide
- Validation user guide
- Free access to bug fixes, optimizations and feature improvements.

ORDERING INFORMATION

The core can be purchased directly from the A3. Visit www.automate.org for more information or use QR code below .

VISION & IMAGING